AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions, and listings, of claims in the application.

Listing of Claims:

1. (Currently Amended) An image display apparatus comprising:

a plurality of signal lines;

a plurality of display pixels arranged in a matrix to provide image display, each of said display pixels comprising a pixel electrode ~~and~~ connected to said each of the plurality of signal lines via a pixel switch ~~connected to said pixel electrode in series~~;

a plurality of data lines;

a plurality of memory ~~elements~~ cells for storing digital display data;

an image signal generating ~~means~~ circuit for outputting ~~a given~~ an image signal to the signal lines based on said digital display data inputted from the plurality of memory cells via the data lines; and

~~a group of signal lines for connecting said image signal generating means to a group of pixel switches; and~~

~~display image selection means for writing said image signal in a given display pixel through said group of signal lines and a group of pixel switches,~~

wherein each ~~basic unit of a~~ the plurality of memory ~~element~~ cells comprises a memory switch; a memory capacitor connected to said memory switch; and ~~an amplifier~~ a field-effect transistor ~~(FET)~~ of which a ~~gate is connected to said memory capacitor;~~ source-drain path thereof is provided between a first node and a second node coupled to a corresponding one of

said data lines, ~~and refreshing operation means for performing a preset refreshing operation to rewrite a signal charge stored in said memory capacitor using said amplifier FET.~~

wherein one electrode of said memory capacitor is connected to a gate of said field-effect transistor and another electrode of said memory capacitor is connected to said second node, and

wherein when a memory cell is read or written, a predetermined voltage is supplied to said first node.

2. (Original) An image display apparatus according to claim 1, wherein each of said plurality of display pixels is a liquid crystal display pixel having a counter electrode and a liquid crystal region between said pixel electrode and said counter electrode.

3. (Original) An image display apparatus according to claim 2, wherein said plurality of display pixels have an optical reflecting plate.

4. (Currently Amended) An image display apparatus according to claim 1, wherein said plurality of display pixels, said ~~group~~ plurality of signal lines and said image signal generating ~~means~~ circuit are formed on a single transparent substrate.

5-8. (Cancelled)

9. (Currently Amended) An image display apparatus according to claim 1, wherein said memory capacitor is a capacitor between a gate and a channel of said ~~amplifier FET~~ field-effect transistor.

10. (Currently Amended) An image display apparatus according to claim ~~6~~1, wherein said memory capacitor is a capacitor between a gate and a channel of a polycrystalline Si thin-film transistor (poly-Si TFT).

11-16. (Cancelled)

17. (Currently Amended) An image display apparatus according to claim 1, wherein ~~a plurality of basic units~~ some of said memory ~~elements~~cells are connected to one ~~another by a~~ data line, and said ~~amplifier FET~~ second node is connected to said corresponding data line through a selection switch.

18. (Cancelled)

19. (Currently Amended) An image display apparatus according to claim ~~18~~17, wherein said selection switch is a polycrystalline Si thin-film transistor (poly-Si TFT) which is diode-connected in which the drain and the gate thereof are directly coupled.

20. (Original) An image display apparatus according to claim 17, wherein said selection switch is a p-n junction diode using a polycrystalline Si thin film.

21-22. (Cancelled)

23. (Currently Amended) An image display apparatus according to claim 17, wherein said ~~basic units of the~~ memory ~~elements~~ cells are arranged in a matrix along ~~a group of~~ said data lines extending in a y-direction, and said data lines are arranged by n line units in a case where unit digital display data composed of n bits is stored by n ~~basic units~~ of said memory ~~elements~~ cells.

24. (Currently Amended) An image display apparatus according to claim 4, wherein lighting means to the display pixels is provided on a surface of said transparent substrate opposite to the surface on which the display pixels, the ~~group~~ plurality of signal lines and the image signal generating ~~means~~ circuit are arranged, and black matrix shielding ~~means~~ is arranged between said transparent substrate corresponding to back portions of said memory ~~elements~~ calls and said lighting means.

25. (Cancelled)

26. (Currently Amended) An image display apparatus according to claim 1, wherein said image signal generating ~~means~~ circuit has digital-to-analog ~~converting means~~ converter for generating an image signal from display data stored in said memory ~~element~~ cell.

27. (Currently Amended) An image display apparatus according to claim 2, wherein said image signal generating ~~means~~ circuit has digital-to-analog ~~converting means~~ converter for generating an image signal from said digital display data stored in said memory ~~element~~ cell, and said digital-to-analog ~~converting means~~ converter has a function of selectively outputting substantially two kinds of image signal voltages to the same digital display data.

28. (Currently Amended) An image display apparatus comprising:

a plurality of display pixels arranged in a matrix in order to provide image display, each display pixel comprising a pixel electrode and a pixel switch connected to said pixel electrode in series;

~~image signal generating means~~ a digital-to-analog converter for outputting an image signal based on digital display data;

a group of signal lines for connecting said ~~image signal generating means~~ digital-to-analog converter to a group of pixel switches; and

display image selection means for writing said image signal in a given display pixel through said group of signal lines and said group of pixel switches,

at least said plurality of display pixels, said group of signal lines and said ~~image signal generating means~~ digital-to-analog converter being formed on a single transparent substrate,

wherein said ~~image signal generating means~~ digital-to-analog converter contains ~~has~~ a reference voltage generating circuit using a boron-doped polycrystalline Si (poly-Si) thin-film resistor as a gray scale voltage generating resistor.

29-39. (Cancelled)